

Constructive Computer Architecture

# Combinational ALU

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L03-1

## Outline

- ◆ Building complex combinational circuits in pieces
- ◆ Parameterization that goes beyond data path widths

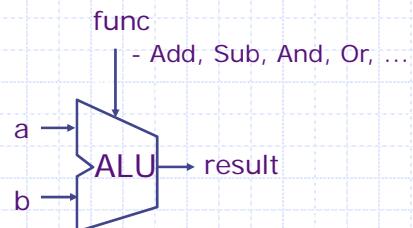
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L03-2

# Arithmetic-Logic Unit (ALU)

ALU performs all the arithmetic and logical functions



```
function Data alu(Data a, Data b,  
                  AluFunc func);
```

Each individual function can be described as a combinational circuit and these can be combined together to produce a combinational ALU

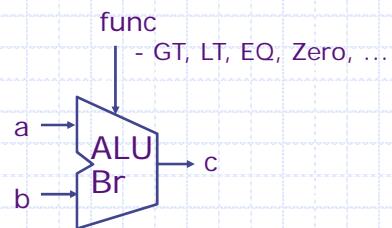
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L03-3

# ALU for comparison operators

Like ALU but returns a Bool



```
function Bool aluBr(Data a, Data b,  
                     BrFunc func);
```

what does func look like?

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# Enumerated types

- ◆ Suppose we have a variable c whose values can represent three different colors
  - Declare the type of c to be Bit#(2) and adopt the convention that 00 represents Red, 01 Blue and 10 Green
- ◆ A better way is to create a new type called Color:

```
typedef enum {Red, Blue, Green}  
Color deriving(Bits, Eq);
```

BSV compiler automatically assigns a bit representation to the three colors and provides a function to test if the two colors are equal

If you do not use "deriving" then  
you will have to specify your own  
encoding and equality function

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# Enumerated types

```
typedef enum {Red, Blue, Green}  
Color deriving(Bits, Eq);  
  
typedef enum {Add, Sub, And, Or, Xor, Nor, Slt, Sltu,  
LShift, RShift, Sra} AluFunc deriving(Bits, Eq);  
  
typedef enum {Eq, Neq, Le, Lt, Ge, Gt, AT, NT}  
BrFunc deriving(Bits, Eq);
```

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L03-6

# Combinational ALU

```
function Data alu(Data a, Data b, AluFunc func);
    Data res = case(func)
        Add   : addN(a,b);
        Sub   : subN(a,b);
        And   : andN(a,b);
        Or    : orN(a,b);
        Xor   : xorN(a,b);
        Nor   : norN(a,b);
        Slt   : zeroExtend(pack(signedLT(a,b)));
        Sltu  : zeroExtend(pack(lt(a,b)));
        LShift: shiftLeft(a,b[4:0]);
        RShift: shiftRight(a,b[4:0]);
        Sra   : signedShiftRight(a,b[4:0]);
    endcase;
    return res;
endfunction
```

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# Comparison operators

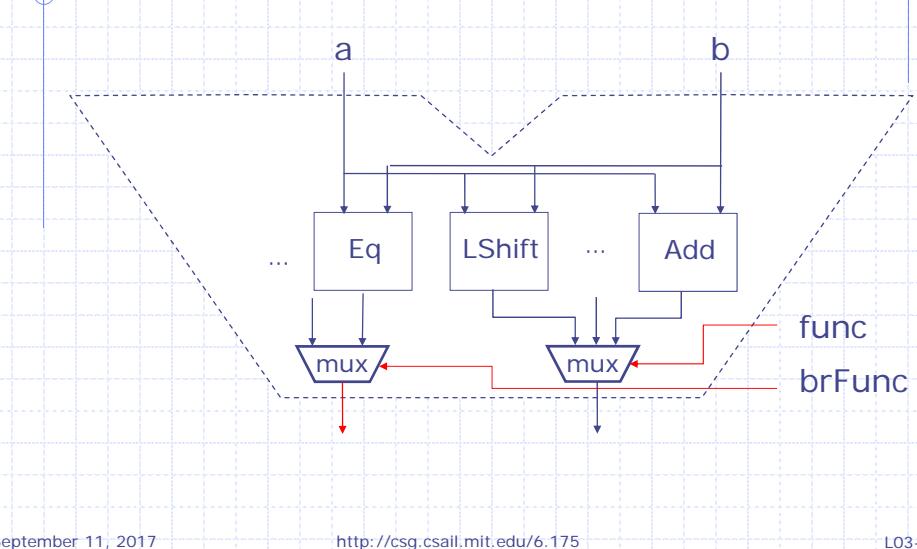
```
function Bool aluBr(Data a, Data b, BrFunc brFunc);
    Bool brTaken = case(brFunc)
        Eq   : (a == b);
        Neq  : (a != b);
        Le   : signedLE(a,b);
        Lt   : signedLT(a,b);
        Ge   : signedGE(a,b);
        Gt   : signedGT(a,b);
        AT   : True;
        NT   : False;
    endcase;
    return brTaken;
endfunction
```

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## ALU including Comparison operators



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## Selectors and Multiplexers

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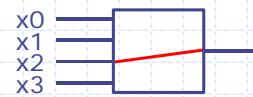
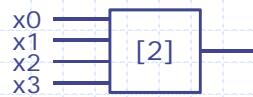
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L03-10

## Selecting a wire: $x[i]$

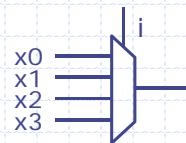
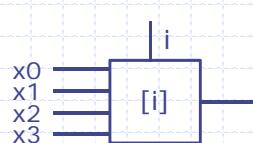
assume  $x$  is 4 bits wide

- Constant Selector: e.g.,  $x[2]$



no hardware;  
 $x[2]$  is just  
the name of  
a wire

- Dynamic selector:  $x[i]$

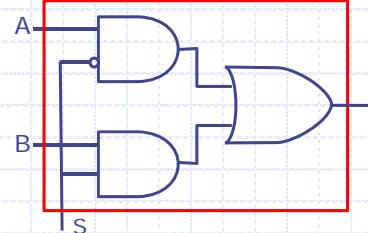
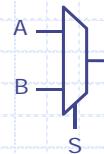


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L03-11

## A 2-way multiplexer



$(S == 0) ? A : B ;$

Gate-level implementation

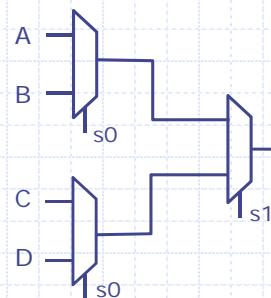
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## A 4-way multiplexer

```
case ({s1,s0}) matches
  0: A;
  1: B;
  2: C;
  3: D;
endcase
```



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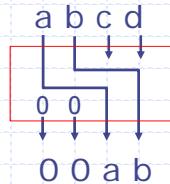
## Shift operators

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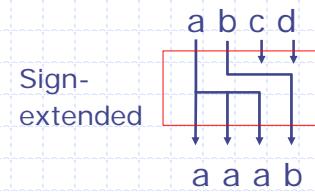
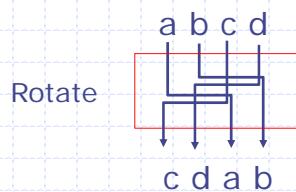
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L03-14

## Logical right shift by 2



- ◆ Fixed size shift operation is cheap in hardware
  - just wire the circuit appropriately
- ◆ Other types of shifts are similar



Sign extension  
is useful for  
converting  
say, a 32-bit  
integer into a  
64-bit integer

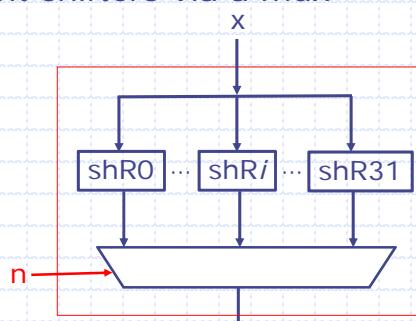
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## Logical right shift by $n$

- ◆ Suppose we want to build a shifter which shift a value  $x$  by  $n$  where  $n$  is between 0 and 31
- ◆ One way to do this is by connecting 31 different shifters via a mux



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## Logical right shift by $n$

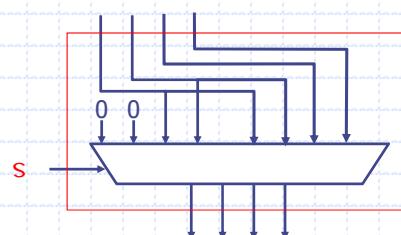
- ◆ Shift  $n$  can be broken down in  $\log n$  steps of fixed-length shifts of size 1, 2, 4, ...
  - For example, we can perform Shift 3 ( $=2+1$ ) by doing shifts of size 2 and 1
  - Shift 5 ( $=4+1$ ) by doing shifts of size 4 and 1
  - Shift 21 ( $=16+4+1$ ) by doing shifts of size 16, 4 and 1
- ◆ For a 32-bit number, a 5-bit  $n$  can specify all the needed shifts
  - $3_{10} = 00011_2$ ,  $5_{10} = 00101_2$ ,  $21_{10} = 10101_2$
- ◆ The bit encoding of  $n$  tells us which shifters are needed; if the value of the  $i^{th}$  (least significant) bit is 1 then we need to shift by  $2^i$  bits

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## Conditional operation: shift versus no-shift



- ◆ We need a mux to select the appropriate wires: if  $s$  is one the mux will select the wires on the left otherwise it would select wires on the right

```
(s==0)?{a,b,c,d}:{0,0,a,b};
```

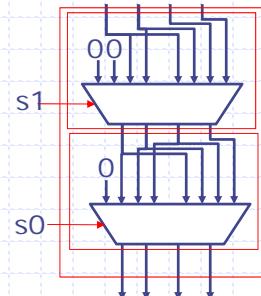
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## Logical right shift ckt

- ◆ Define  $\log n$  shifters of sizes 1, 2, 4, ...
- ◆ Define  $\log n$  muxes to perform a particular size shift
- ◆ Shift circuit can be expressed as  $\log n$  nested conditional expressions where  $s_0, s_1 \dots$  Represent the bits of  $n$



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## Complex Combinational Circuits

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## Multiplication by repeated addition

$$\begin{array}{rcl} b \text{ Multiplicand} & 1101 & (13) \\ a \text{ Multiplier} & * \quad 1011 & (11) \\ & 0000 \\ & \underline{x \quad 1101} \\ m_0 & 1101 \\ m_1 & + \quad 1101 \\ m_2 & + \quad 0000 \\ m_3 & + \quad 1101 \\ & \underline{10001111 \quad (143)} \end{array}$$

At each step we add either 1101 or 0 to the result depending upon a bit in the multiplier

`mi = (a[i]==0)? 0 : b;`

We also shift the result by one position at every step

However, our addN circuit adds only two numbers at a time!

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## Multiplication by repeated addition *cont.*

$$\begin{array}{rcl} b \text{ Multiplicand} & 1101 & (13) \\ a \text{ Multiplier} & * \quad 1011 & (11) \\ & 0000 \\ t_0 & + \quad 1101 \\ t_1 & \underline{+ \quad 01101} \\ m_1 & + \quad 1101 \\ t_2 & \underline{\quad \quad \quad \quad} \\ m_2 & \underline{\quad \quad \quad \quad} \\ t_3 & \underline{\quad \quad \quad \quad} \\ m_3 & \underline{\quad \quad \quad \quad} \\ t_4 & \underline{\quad \quad \quad \quad} \end{array}$$

At each step we add either 1101 or 0 to the result depending upon a bit in the multiplier

`mi = (a[i]==0)? 0 : b;`

We also shift the result by one position at every step

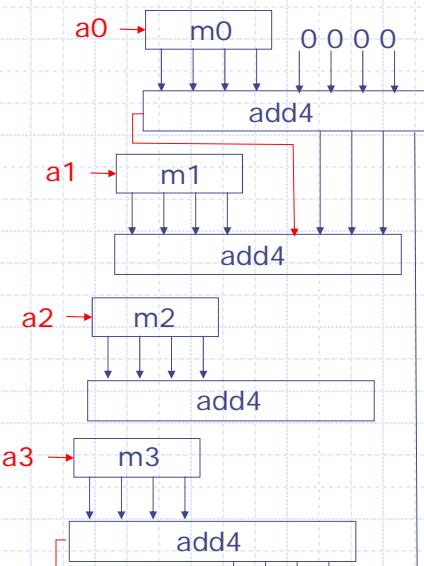
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## Multiplication by repeated addition ckt

$$\begin{array}{r}
 \begin{array}{l}
 \text{b Multiplicand} \quad 1101 \quad (13) \\
 \text{a Multiplier} \quad * \quad 1011 \quad (11) \\
 \hline
 \text{tp} \quad 0000 \\
 \text{m0} \quad + \quad 1101 \\
 \hline
 \text{tp} \quad 01101 \\
 \text{m1} \quad + \quad 1101 \\
 \hline
 \text{tp} \quad 100111 \\
 \text{m2} \quad + \quad 0000 \\
 \hline
 \text{tp} \quad 0100111 \\
 \text{m3} \quad + \quad 1101 \\
 \hline
 \text{tp} \quad 10001111 \quad (143)
 \end{array} \\
 \boxed{\text{mi} = (\text{a}[i]==0)? 0 : \text{b};}
 \end{array}$$



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L03-23

## Combinational 32-bit multiply

```

function Bit#(64) mul32(Bit#(32) a, Bit#(32) b);
    Bit#(32) tp = 0;
    Bit#(32) prod = 0;
    for(Integer i = 0; i < 32; i = i+1)
        begin
            Bit#(32) m = (a[i]==0)? 0 : b;
            Bit#(32) sum = add32(m, tp, 0);
            prod[i] = sum[0];
            tp = sum[32:1];
        end
    return {tp,prod};
endfunction
  
```

### ◆ Long chains of gates

- 32-bit multiply has 32 ripple carry adders in sequence!
- 32-bit ripple carry adder has a 32-long chain of gates

### ▪ Total delay ?

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